ROBO-505

Single Board Computer

User's Manual

P/N : 861105080008 Version 1.0

Copyright © Portwell, Inc., 1998. All rights reserved.
All other brand names are registered trademarks of their respective owners.

EC Declaration of Conformity

(To Be Added)

For the following equipment :

Product Name :

Model Name :

Trade Name :

is herewith confirmed to comply with the requirements set out in the Council Directive on the Approximation of the Laws of the Member States relating to Electromagnetic Compatibility Directive (89/336/EEC). The equipment was evaluated and passed the test, the following standards were applied :

EMC :	EN 55022	(1994/A1:1995 Class A)
	EN 50082-2	(1991)
	EN 61000-4-2	(1995)
	EN 61000-4-3	(1996)
	EN 61000-4-4	(1995)
	EN 61000-3-2	(1995)
	EN 61000-3-3	(1995)

The following manufacturer is responsible for this declaration :

Portwell Inc.

(Company Name)

(Company Address)

Taipei, R.O.C.

Place	Date	Legal Signature of Authorized Person

Table of Contents

How to Use This Manual

Chapter 1. Introduction

1.1 Check List 1-2
1.2 Product Specifications 1-3
1.3 System Architecture 1-6

Chapter 2. Hardware Configuration Setting

2.1 Jumpers .....2 – 1
2.2 Connectors .....2 – 6

Chapter 3. System Installation

3.1 Socket 7 Processor .....3 – 1
3.2 Main Memory .....3 – 1
3.3 M-system Flash Disk .....3 – 2
3.4 Installing the Single Board Computer .....3 – 2
3.4.1 CHIPS 69000 Graphics Controller .....3 – 2
3.4.2 LCD Panel Interface Kit .....3 – 2
3.4.3 RTL8139 Fast Ethernet Controller .....3 – 2
3.4.4 On-board LED Indicator .....3 – 2
3.4.5 Drivers Support .....3 – 2
3.5 Watch Dog Timer Programming .....3 – 3

Chapter 4. BIOS Setup Information

4.1 Entering Setup .....4 – 1
4.2 Main Menu .....4 – 2
4.3 Standard CMOS Setup Menu .....4 – 3
4.4 Advanced CMOS Setup Menu ..... 4 – 3
4.5 Advanced Chipset Setup Menu .....4 – 5
4.6 Power Management Setup Menu .....4 – 7
4.7 PCI/Plug and Play Setup Menu .....4 – 10
4.8 Peripheral Setup Menu .....4 – 12
4.9 Hardware Monitor Menu .....4 – 14
4.10 BIOS POST Check Point List .....4 – 15
4.11 Flash BIOS Utility .....4 – 20

How to Use This Manual

The manual describes how to configure your ROBO-505 system to meet various operating requirements. It is divided into four chapters, with each chapter addressing a basic concept and operation of Single Board Computer.

Chapter 1 : Introduction. presents what you have in the inside of box and give you an overview of the product specifications and basic system architecture for this model of single board computer.

Chapter 2 : Hardware Configuration Setting. shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. describes how to properly mount the CPU and main memory, M-system Flash disk, or optional flat panel display interface module to get a safe installation and give you a programming guide of Watch Dog Timer function. Besides, it will introduce and show you the driver installation procedure about Graphics Controller and Ethernet Controller.

Chapter 4 : BIOS Setup Information. specifies the meaning of each setup parameters and how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give you a guide of trouble-shooting.

The content of this manual and EC declaration document is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site :
http://www.portwell.com

CHAPTER 1

Introduction

The ROBO-505 all-in-one half-sized single board computer is designed to fit a high performance Pentium-based CPU and compatible for computer system with ISA bus architecture. The on-board PCI bus supports two PCI devices--, VGA with versatile flat panel interface and Ethernet function. It is made to meet today's demanding pace, and keep complete hardware and software compatibility with the IBM PC/AT. It's beneficial to build up a high performance and high data availability system for VARs, or system integrators. The on-board PCI-bus graphics controller with panel support and the fast Ethernet interface will bring full functionality and high performance to the PC market.

This single board computer can run with Intel Pentium or compatible processor up to 333 MHz, support 512KB L2 cache and DIMM up to 128MB DRAM. The enhanced on-board PCI IDE interface can support two drives up to PIO mode 4 timing and Ultra DMA/33 synchronous mode feature. Two on-board USB (Universal Serial Bus) ports provide high-speed data communication for USB peripherals. The Super I/O Chipset integrates floppy controller, two standard serial ports, one IrDA (Standard & Fast Infrared) port and one parallel port. Two high performance 16C550-compatible UARTs provide 16-byte send/receive FIFOs, and the multi-mode parallel port supports SPP/EPP/ECP function. Besides, it also appends one I/O chipset to support another two serial ports.

The on-board 32-pin DIP socket supports M-system Disk-on-Chip Flash disk up to 144MB. Built-in Watch-dog Timer function to monitor your system status. Two 6-pin Mini-DIN connectors are provided to connect PS/2 mouse and keyboard. The on-board Flash ROM is used to make the BIOS update easier. A standard P8 power connector is reserved to support embedded platform, the additional 5-pin shrouded connector is reserved for connecting keyboard interface on the backplane. The high precision Real Time Clock/calendar is built in for accurate scheduling and system configuration storage. All these features make ROBO-505 excellent in stand-alone applications.

1-1 Check List

The ROBO-505 package includes the following basic items accompany with this manual.

- One ROBO-505 single board computer
- One Parallel port cable
- Two serial port cables to support four interfaces
- One FDC cable
- One IDE cable
- One 5-pin to 5-pin keyboard cable for backplane connection
- One CD-title to support VGA and Ethernet drivers

If any of these items is damaged or missed, please contact your vendor and save all packing materials for future replacement and maintenance.

1-2 Product Specifications

- **Main processor**
  Intel Pentium P54C/P55C, AMD K5/K6/K6-2 series, Cyrix M1/M2 series or compatible up to 333 MHz
  ◇ CPU bus clock : 60/66 MHz
  ◇ CPU core/bus clock ratio : X1.5 to X5.5
  ◇ CPU Vcore Voltage : 1.8V to 3.5V

- **BIOS**
  AMI system BIOS with 256KB Flash ROM

- **Main Memory**
  One 168-pin DIMM socket, supporting 3.3V SDRAM or EDO DRAM up to 128MB

- **L2 Cache Memory**
  On-board 512KB Pipeline Burst Static RAM and 64MB DRAM Cacheability

- **Chipset**
  Intel 82430TX PCIset

- **Bus Interface**
  Follow 16-bit ISA bus standard

- **PCI IDE Interface**
  Supports one enhanced IDE port up to two HDD devices with PIO mode 4 and Ultra DMA/33 mode 2 timing transfer

- **Floppy Drive Interface**
  Supports one FDD port up to two floppy drives and 5-1/4"(360K, 1.2MB), 3-1/2" (720K, 1.2MB, 1.44MB, 2.88MB) diskettes

- **Serial Ports**
  Support four high-speed serial ports with 16-byte FIFOs

- **IR Interface**
  Supports one 6-pin header for serial Standard/Fast Infrared wireless communication

- **Parallel Port**
  Supports one SPP, EPP/ECP bi-directional parallel port

- **USB Interface**
  Supports two USB ports for high speed I/O peripheral devices with USB interface

- **PS/2 Mouse and Keyboard Interface**
  Supports two 6-pin Mini-DIN connectors and one 5-pin shrouded connector for PS/2 mouse, keyboard and backplane connection

- **Auxiliary I/O Interfaces**
  System reset switch, external speaker, Keyboard lock and HDD LED interface

- **Real Time Clock/Calendar (RTC)**
  Real Time Clock/calendar with battery backup for 10-year data retention

- **Watchdog Timer**
  0.5,1,2,4,8,16,32,64 sec. time-out intervals by jumper setting or 255 intervals from 0.5 min. to 254.5 min. by software programming from I/O chipset

- **Disk-On-Chip (DOC) Feature**
  Reserved one 32-pin sockets for M-system Flash Disk up to 144MB

- **On-board VGA and flat panel interface**
  Adapts CHIPS 69000 HiQVideo Accelerator with integrated memory (2MB or 4MB) to provide high performance graphics and panel display capabilities

- **Optional panel display interface module**
  Reserved one 40-pin header for panel display adapter to support DSTN/Mono/TFT with LVDS technology

- **On-board Ethernet**
  Utilizes Realtek RTL8139A Fast Ethernet Controller to support RJ-45 interface with 10/100BASE-T operation

- **CPU Temperature Control**
  Automatically control CPU speed to prevent it from over heating

- **High Driving Capability**
  Supports high driving capability for multi-slots ISA-bus

- **External Power Connector**
  Supports one standard P8 power connector to support stand-alone application

- **Power Good**
  On-board power good generator with reset time, 300ms ～ 500ms

- **Physical and Environmental Requirements**
  - ◆ Outline Dimension (L X W) : 339.5mm (13.36”) X 121.5mm (4.78”)
  - ◆ Board Weight : 0.55 lb. (0.25kg)
  - ◆ PCB layout : 8 layer
  - ◆ Power Requirements : +5V @5.0A (typ.), +12V @60mA, -12V @60mA
  - ◆ Operating Temperature : 0℃ ～ 60℃ (32℉ ～ 140℉)
  - ◆ Storage Temperature : -20℃ ～ 80℃
  - ◆ Relative Humidity : 5% ～ 95%, non-condensing

1-3 System Architecture

The following illustration of block diagram will show you how does ROBO-505 give you a highly integrated system solution. The most up-to-date system architecture of ROBO-505 is based on Intel 430TX PCIset , which consists of the 82439TX System Controller (MTXC) and the 82371AB PCI ISA IDE Xcelerator (PIIX4). This equips ROBO-505 to support Pentium Processor, SDRAM, PBSRAM L2 Cache, PCI bus interface, ACPI compliant power management, USB port, SMBus communication, and Ultra DMA/33 IDE Master. The on-board super I/O chip, W83977ATF, will support PS/2 Keyboard/Mouse, two UARTs, FDC, Parallel and Infrared interface. Another I/O chip, W83877TF, supports two extra standard serial interfaces. In addition, the on-board Graphics Controller with optional panel display support and LAN interface will give user more flexibility and reliability in a harsh environment.

The North Bridge 82439TX provides a completely integrated solution for the system controller and data path components in a Pentium processor system. The MTXC supports all compatible Pentium family processors since P54C. It has 64-bit Host and DRAM Bus Interface, 32-bit PCI bus interface, second level cache interface with 64MB DRAM cacheability, and supports two on-board PCI devices, LAN and VGA with panel solution.

The South Bridge, 82371AB, provides a highly integrated multifunction PCI-to-ISA bridge solution for the best industry application. It supports 2-channel dedicated Ultra DMA/33 IDE master interfaces, full Plug-and-Play compatibility, and APIC (Advanced Programmable Interrupt Controller) interface. It also supports 2-port USB (Universal Serial Bus feature) and PCI 2.1 Compliance operation. It fully supports Operating System Directed Power Management via the Advanced Configuration and Power Interface (ACPI) specification. In addition, it also provides XD-bus via buffer logic control to support BIOS read/write access and external real-time clock (RTC) to maintain date and time of a system.

The Super I/O chip W83977ATF, which integrates two high-speed serial ports, one parallel port, FIR/SIR interface, 8042 keyboard controller with PS/2 mouse ports and FDD interface. This parallel port supports one PC-compatible Standard Printer Port (SPP), Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Another I/O chip W83877TF also supports two standard serial interfaces to obtain four COM ports in all for ROBO-505.

Two 16-bit ISA-bus interfaces, standard ISA and PC/104 bus, are applied for all of slower I/O operations. In ROBO-505, it contains Watch-dog Timer (WDT) enabled by jumper setting and triggered by software, Disk-on-Chip (DOC) for M-system Flash disk, and ISA buffer driving for special I/O applications and multi-ISA slots. The detail operating relations are shown in Figure 1-1 ROBO-505 System Block Diagram.

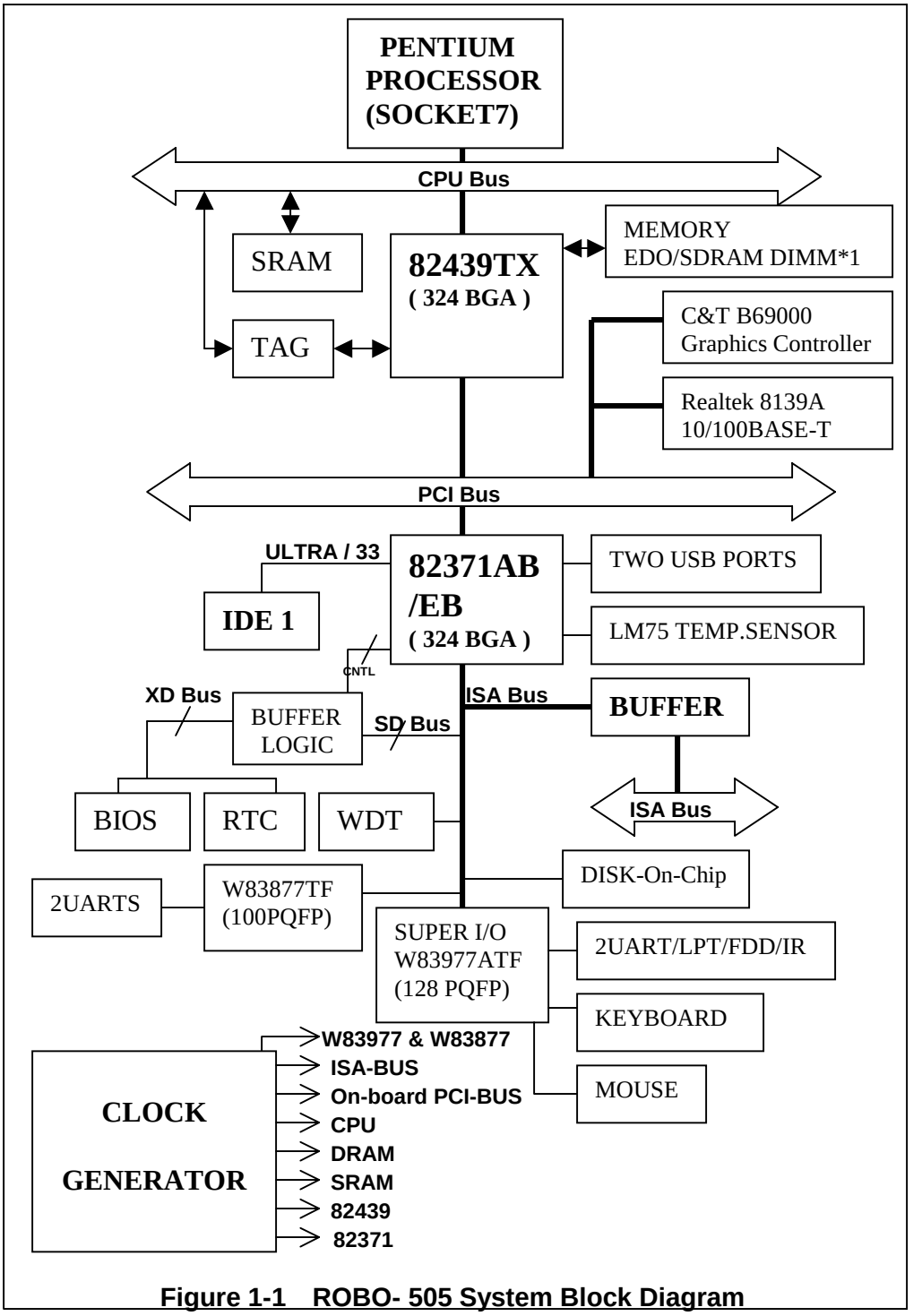


Figure 1-1 ROBO- 505 System Block Diagram

CHAPTER 2

Hardware Configuration Setting

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on ROBO-505 are properly set. The factory default settings are marked with a star (★).

2-1 Jumpers

In general, jumpers on the single board computer are used to select options for certain features. Some of the jumpers are user-configurable, which allows system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (Short) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connected". (Please refer to Figure 2-1 for detail jumper positions)

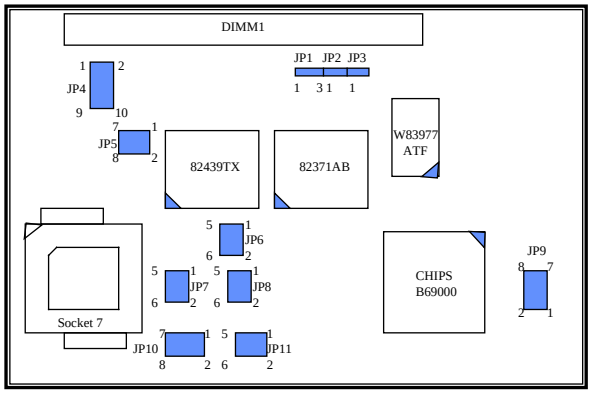


Figure 2-1 ROBO-505 Jumper Locations

CPU Jumper Setting Table (JP4, JP5, JP1, JP7, JP8)

(A) JP4, JP5 CPU Voltage Selection

JP4 : CPU Vcore/Vcc2

9 – 10	7 – 8	5 – 6	3 – 4	1 – 2	Vcore Voltage
NC	NC	NC	NC	NC	2.00 V
NC	NC	NC	NC	Short	2.10 V
NC	NC	NC	Short	NC	2.20 V ★
NC	NC	NC	Short	Short	2.30 V
NC	NC	Short	NC	NC	2.40 V
NC	NC	Short	NC	Short	2.50 V
NC	NC	Short	Short	NC	2.60 V
NC	NC	Short	Short	Short	2.70 V
NC	Short	NC	NC	NC	2.80 V
NC	Short	NC	NC	Short	2.90 V
NC	Short	NC	Short	NC	3.00 V
NC	Short	NC	Short	Short	3.10 V
NC	Short	Short	NC	NC	3.20 V
NC	Short	Short	NC	Short	3.30 V
NC	Short	Short	Short	NC	3.40 V
NC	Short	Short	Short	Short	3.50 V
Short	NC	NC	NC	NC	1.80 V
Short	NC	NC	NC	Short	1.90 V
Short	NC	NC	Short	NC	2.00 V
Short	NC	NC	Short	Short	2.10 V
Short	NC	Short	NC	NC	2.20 V
Short	NC	Short	NC	Short	2.30 V
Short	NC	Short	Short	NC	2.40 V
Short	NC	Short	Short	Short	2.50 V
Short	Short	NC	NC	NC	2.80 V
Short	Short	NC	NC	Short	2.90 V
Short	Short	NC	Short	NC	3.00 V
Short	Short	NC	Short	Short	3.10 V
Short	Short	Short	NC	NC	3.20 V
Short	Short	Short	NC	Short	3.30 V
Short	Short	Short	Short	NC	3.40 V
Short	Short	Short	Short	Short	3.50 V

JP5 : CPU Vio/Vcc3

Jumper Location	CPU Voltage Type
1 – 2 , 3 – 4	Dual Voltage ★
5 – 6 , 7 – 8	Single Voltage

NOTE : JP5 is used to choose single or dual voltage for CPU, you can easily see the right voltage label on CPU surface marking.

■ Reference Table for various CPU settings : **(Reference Only)**

CPU TYPE	JP4	JP5	Vcore	Vio
Single Voltage **INTEL** P54C/CQS/CT **Cyrix** 6x86 **AMD** K5	1-2 Short 3-4 Short 5-6 Short 7-8 Short	5-6 Short 7-8 Short	3.5V	3.5V
Dual Voltage **INTEL** P55C/MMX **Cyrix** 6x86L (M1L)	7-8 Short	1-2 Short 3-4 Short	2.8V	3.3V
AMD K6-166/200 **Cyrix** 6x86MX (M2)	1-2 Short 7-8 Short	1-2 Short 3-4 Short	2.9V	3.3V
AMD K6-233	5-6 Short 7-8 Short	1-2 Short 3-4 Short	3.2V	3.3V
AMD K6-2/3D ★	3-4 Short	1-2 Short 3-4 Short	2.2V	3.3V

(B) JP1, JP7, JP8 CPU Clock Selection

B-1. JP8 specifies system bus frequency

5-6	3-4	1-2	CPU Bus Clock	PCI Bus Clock	Remark
Short	Short	Short	50 MHz	25 MHz	
NC	Short	NC	75 MHz	37.5 MHz	
NC	NC	Short	60 MHz	30 MHz	
NC	NC	NC	66.8 MHz ★	33.4 MHz	

B-2. JP7 specifies CPU core/bus ratio

1-2	3-4	5-6	Core/Bus Ratio
Short	NC	NC	2.0X
Short	Short	NC	2.5X
NC	Short	NC	3.0X
NC	NC	NC	1.5X or 3.5X
Short	NC	Short	4.0X
Short	Short	Short	4.5X ★
NC	Short	Short	5.0X
NC	NC	Short	5.5X

NOTE :

(1) The currently foregoing JP8/JP9/JP10/JP12 settings are dedicated for AMD K6-2/3D 300MHz CPU.

(2) For system stability, don't arbitrarily over speed your CPU.

B-3. JP1 specifies bus frequency detection of Host Bridge MTXC

JP1	Bus Frequency
1 – 2	66 MHz , (75 MHz) ★
2 – 3	60 MHz , (50 MHz)

RTC CMOS Clear Jumper Setting (JP3)

JP3 NC : Normal operation ★
Short : Clear CMOS contents

NOTE : In general, CMOS clearing operation can be done under system power on if CMOS RAM CLEAR FUNCTION does not exist in the BIOS Advanced Chipset Setup. For certain RTC supports hardware Y2K, it also can be done under system power on or off. Here please make sure that the CMOS RAM clear option has been enabled in Advanced Chipset Setup before CMOS clearing happens.

Disk-On-Chip Jumper Setting (JP10)

Address mapping of memory window

1 – 2	3 – 4	5 – 6	7 – 8	Memory Address Space
Short	NC	NC	NC	C0000 – C7FFF
NC	Short	NC	NC	C8000 – CFFFF
NC	NC	Short	NC	D0000 – D7FFF ★
NC	NC	NC	Short	D8000 – DFFFF

Watch-Dog Timer Jumper Setting (JP6, JP11,JP2)

JP6 1 – 3 (or 3 – 4) : System reset will be triggered by H/W WDT timeout
2 – 4 (or 1 – 2): Disconnected WDT output to system reset
(i.e. WDT function is disabled) ★
3 – 5 : Connect H/W WDT output to NMI
4 – 6 : System reset will be triggered by S/W WDT (initiated and programmed by software from super I/O chipset)

JP2 NC : Allocate I/O port 0433h/0033h for H/W WDT programming ★
Short : Allocate I/O port 0443h/0343h for H/W WDT programming

JP11 WDT Time-out Interval

5-6	3-4	1-2	TIME-OUT INTERVAL
Short	Short	Short	0.5 sec.
Short	Short	NC	1 sec. ★
Short	NC	Short	2 sec.
Short	NC	NC	4 sec.
NC	Short	Short	8 sec.
NC	Short	NC	16 sec.
NC	NC	Short	32 sec.
NC	NC	NC	64 sec.

Optional LCD Panel Type Jumper Setting (JP9)

JP9 : Flat Panel Type

7 – 8	5 – 6	3 – 4	1 – 2	Flat Panel Type
Short	Short	Short	Short	1024x768 Dual Scan STN Color Panel →reserved
Short	Short	Short	NC	1280x1024 TFT Color Panel →reserved
Short	Short	NC	Short	640x480 Dual Scan STN Color Panel →reserved
Short	Short	NC	NC	800x600 Dual Scan STN Color Panel →reserved
Short	NC	Short	Short	640x480 Sharp TFT Color Panel →reserved
Short	NC	Short	NC	640x480 18-bit TFT Color Panel
Short	NC	NC	Short	1024x768 TFT Color Panel
Short	NC	NC	NC	800x600 TFT Color Panel
NC	Short	Short	Short	800x600 TFT Color Panel (L. BIOS) →reserved
NC	Short	Short	NC	800x600 TFT Color Panel (L. BIOS)
NC	Short	NC	Short	800x600 Dual Scan STN Color Panel (L. BIOS) →reserved
NC	Short	NC	NC	800x600 Dual Scan STN Color Panel (L. BIOS) →reserved
NC	NC	Short	Short	1024x768 TFT Color Panel (L. BIOS) →reserved
NC	NC	Short	NC	1280x1024 Dual Scan STN Color Panel (L. BIOS)→reserved
NC	NC	NC	Short	1024x600 Dual Scan STN Color Panel (L. BIOS) →reserved
NC	NC	NC	NC	1024x600 TFT Color Panel (Large BIOS)

NOTE : This jumper JP9 is available only for flat panel installation.

2-2 Connectors

I/O peripheral devices and Flash disk will be connected to these interface connectors or DOC socket located on this single board computer.

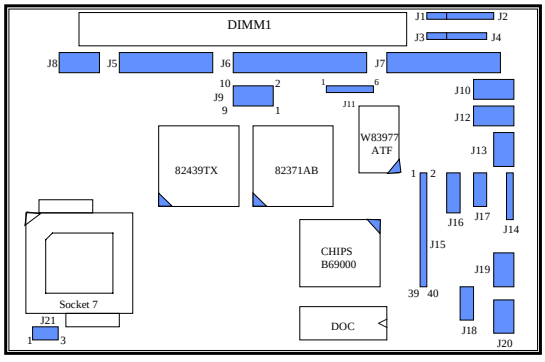


Figure 2-2 ROBO-505 Connector Locations

CONNECTOR	FUNCTION	REMARK
J1	System reset	
J2	Keyboard lock and power indicator	
J3	IDE1/IDE2 active LED interface	
J4	External speaker interface	
J5	Parallel port connector	
J6	IDE1 (Primary) interface	
J7	Floppy connector	
J8	Standard P8 power connector	
J9	External USB interface	Support two ports
J10	COM1 serial port	DSUB-9
J11	IrDA (infrared) port	Support FIR/SIR
J12	COM2 serial port	2 x 5 shrouded header
J13	LAN interface connector	RJ-45 port
J14	VGA connector	DSUB-15
J15	Flat Panel display module interface	2x20 pin header
J16	COM3 serial port	2x5 shrouded header
J17	COM4 serial port	2x5 shrouded header
J18	External keyboard interface	Connect to backplane
J19	PS/2 mouse connector	6-pin Mini-DIN
J20	PS/2 keyboard connector	6-pin Mini-DIN
J21	CPU cooling fan power connector	Support +12V
U13	On-board Flash disk (Disk-On-Chip)	32-pin DIP socket

Pin Assignments of Connectors

■ **J1 : Reset Header**

PIN No.	Signal Description
1	Reset
2	Ground

■ **J2 : Keyboard Lock Header**

PIN No.	Signal Description
1	+5V (330 ohm pull-up for power LED)
2	N/C
3	Ground
4	Keyboard inhibit
5	Ground

■ **J3 : IDE1/IDE2 Active LED Header**

PIN No.	Signal Description
1	+5V (470 ohm pull-up for HDD LED)
2	HDD Active # (LED cathode terminal)

■ **J4 : External Speaker Header**

PIN No.	Signal Description
1	Speaker signal
2	N/C
3	Ground
4	+5V

■ **J8 : Standard P8 Power Connector**

PIN No.	Signal Description
1	N/C
2	+5V
3	+12V
4	-12V
5	Ground
6	Ground

■ **J5 : Parallel Port Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	Strobe#	14	Auto Form Feed#
2	Data 0	15	Error#
3	Data 1	16	Initialization#
4	Data 2	17	Printer Select IN#
5	Data 3	18	Ground
6	Data 4	19	Ground
7	Data 5	20	Ground
8	Data 6	21	Ground
9	Data 7	22	Ground
10	Acknowledge#	23	Ground
11	Busy	24	Ground
12	Paper Empty	25	Ground
13	Printer Select	26	N/C

■ **J6 : IDE1 Interface Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	RESET#	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	N/C
21	DMA REQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IOCHRDY	28	Pull-down
29	DMA ACK#	30	Ground
31	INT REQ	32	N/C
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0#	38	HDC CS1#
39	HDD Active#	40	Ground

■ **J7 : FDC Interface Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Density Select
3	Ground	4	N/C
5	Ground	6	N/C
7	Ground	8	Index#
9	Ground	10	Motor ENA#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor ENB#
17	Ground	18	Direction#
19	Ground	20	Step#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 0#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Head Select#
33	Ground	34	Disk Change#

■ **J9 : External USB Interface Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	N/C
3	SBD0- (USBP0-)	4	Ground
5	SBD0+ (USBP0+)	6	SBD1+ (USBP1+)
7	Ground	8	SBD1- (USBP1-)
9	N/C	10	+5V

■ **J10/J12/J16/J17 : Serial Port-1/2/3/4 (2x5 Shrouded Connector)**

PIN	Signal Description	PIN	Signal Description
1	Data Carrier Detect (DCD)	6	Data Set Ready (DSR)
2	Receive Data (RXD)	7	Request to Send (RTS)
3	Transmit Data (TXD)	8	Clear to Send (CTS)
4	Data Terminal Ready (DTR)	9	Ring Indicator (RI)
5	Ground (GND)	10	N/C

■ **J11 : Fast & Standard IrDA Header**

PIN No.	Signal Description
1	VCC (+5V)
2	FIRRX
3	SIRRX
4	Ground
5	IRTX
6	CIRRX (Consumer IR Receiving I/P)

■ **J13 : Ethernet RJ-45 Interface Connector**

PIN No.	Signal Description
1	TX+
2	TX-
3	RX+
4	Termination to Ground
5	Termination to Ground
6	RX-
7	Termination to Ground
8	Termination to Ground

■ **J14 : VGA DSUB-15 Connector**

PIN No.	Signal Description
1	R
2	G
3	B
4	N/C
5	Ground
6	Ground
7	Ground
8	Ground
9	N/C
10	Ground
11	N/C
12	MONID1
13	HSYNC
14	VSYNC
15	MONID2

■ **J15 : Flat Panel Display Module Interface**

PIN No.	Signal Description	PIN No.	Signal Description
1	P0	2	P1
3	P2	4	P3
5	P4	6	P5
7	P6	8	P7
9	P8	10	P9
11	P10	12	P11
13	P12	14	P13
15	P14	16	P15
17	Ground	18	P16
19	SHFCLK	20	P17
21	Ground	22	Ground
23	P18	24	P19
25	P20	26	P21
27	P22	28	P23
29	FLM	30	ENAVEE
31	LP	32	PCLK
33	M	34	+5V
35	+12V	36	+5V
37	+12V	38	+5V
39	Ground	40	Ground

■ **J18 : External Keyboard Connector**

PIN No.	Signal Description
1	Keyboard Clock
2	Keyboard Data
3	N/C
4	Ground
5	+5V

■ **J19 : PS/2 Mouse Connector (6-pin Mini-DIN)**

PIN No.	Signal Description
1	Mouse Data
2	N/C
3	Ground
4	+5V
5	Mouse Clock
6	N/C

■ **J20 : PS/2 Keyboard Connector (6-pin Mini-DIN)**

PIN No.	Signal Description
1	Keyboard Data
2	N/C
3	GND
4	+5V
5	Keyboard Clock
6	N/C

■ **J21 : CPU Cooling FAN Power Connector**

PIN No.	Signal Description
1	+12V
2	Ground
3	N/C

CHAPTER 3

System Installation

This chapter provides you with instructions on how to set up your system. The additional information shows you how to install M-system Flash disk, set up LCD display and handle WDT operation in software program.

3-1 Socket 7 Processor

Installing CPU

1) Align the processor pins with pin holes on the socket. Make sure that the notched corner or dot mark (pin 1) of both CPU and socket are matched. Then press the CPU gently until it fits into place. If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformity.
2) Here the socket is advanced SAZ (Screwdriver Actuated ZIF) type. Put a flat blade screwdriver down to the "lock" hole of the socket. Lever the screwdriver in a horizontal direction to actuate the socket, Be sure that the processor is mated in the socket firmly.
3) Follow the installation guide of cooling fan or heat sink to mount it to the CPU surface and lock it on the socket.
4) Be sure to follow particular CPU speed and voltage type to adjust the jumper settings properly.

Removing CPU

1) Remove the cooling fan first.
2) Put a screwdriver down to the "open" hole of the socket. Lever the screwdriver and follow actuating direction to unmate the processor.
3) Carefully lift up the existing CPU to remove it from the socket.

3-2 Main Memory

This ROBO-505 provides one DIMM (168-pin Dual In-line Memory Module) to support on-board main memory. The maximum memory size for 3.3V EDO DRAM or SDRAM is 128MB. The DIMM used could be either 3.3V EDO (Extended Data Out) memory with speed less than 70ns or 3.3V SDRAM (Synchronized DRAM) with speed less than 100ns.

For system compatibility and stability, don't use memory module without brand. You can also use the single or double-side DIMM without parity check and ECC function.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedure to install your DRAM module into memory socket. Before locking, make sure that the module has been fully inserted into card slot.

NOTE : For maintaining system stability, don't change any of DRAM parameters in BIOS setup to upgrade your system performance except for getting technical information.

3-3 M-system Flash Disk

ROBO-505 reserves one 32-pin DIP sockets for installing M-system Flash disk from 2MB to 144MB. This operation structure is running with pure ISA-bus without PnP (Plug and Play) function. Before installing, make certain that I/O address jumper setting is set on right position to prevent unworkable system due to I/O resource conflict. Do remember to follow DOC (Disk-On-Chip) installation procedure. Otherwise, the Flash chip is possible to be burned out due to incorrect installation.

Installing DOC

Align the DOC with pin holes on the socket. Make sure that the notched corner or dot mark (pin 1) of DOC corresponds to notched corner of the socket. Then press the DOC gently until it fits into place. If installation procedure is correct, the Flash disk can be viewed as a normal hard disk to access read/write data.

WARNING : Please ensure that your DOC is properly inserted. Placing the DOC in reverse will cause severe damage to it.

If you want to boot from this Flash disk, it is necessary to refer to the application note from M-system. You can easily obtain relative information from M-system shipping package (such as product manual) or Web-site **http://www.m-sys.com**.

3-4 Installing the Single Board Computer

To install your ROBO-505 into standard chassis or proprietary environment, you need to perform the following :

- ☐ Step 1 : Check all jumpers setting on proper position
- ☐ Step 2 : Install and configure CPU and memory module on right position
- ☐ Step 3 : Place ROBO-505 into the dedicated position in your system
- ☐ Step 4 : Attach cables to existing peripheral devices and secure it

NOTE : Please refer section 3-4-1, 3-4-2 up to 3-4-5 to install drivers and setup your system.

3-4-1 CHIPS 69000 Graphics Controller

The on-board graphics controller adopts CHIPS 69000 that integrates high performance memory technology for the graphics frame buffer. Based on the proven HiQVideo graphics accelerator core, the 69000 combines state-of-the-art flat panel controller capabilities with low power, high performance integrated memory. It incorporates 2MB of proprietary integrated SDRAM for the graphics/video frame buffer. The integrated SDRAM memory can support up to 83MHz operation, thus increasing the available memory bandwidth for the graphics subsystem to support high color/high resolution application.

The 69000 supports a wide variety of monochrome and color Single-Panel, Single-Drive and Dual-Panel, Dual Drive, standard and high-resolution, passive STN and active matrix TFT/MIM LCD, and EL panels. It is designed to support high performance graphics and video acceleration for all supported display resolutions, display types, and color modes. This PCI device 69000 can configured to operate an analog CRT monitor and flat panel at the same time.

Display Modes Supported

The 69000 supports the modes which appear in the table below.

Resolution	Color (bpp)	Refresh Rates (Hz)
640x480	8	60, 75, 85
640x480	16	60, 75, 85
640x480	24	60, 75, 85
800x600	8	60, 75, 85
800x600	16	60, 75, 85
800x600	24	60, 75, 85
1024x768	8	60, 75, 85
1024x768	16	60, 75, 85
1280x1024	8	60

ROBO-505 utilizes on-board CHIPS 69000 and optional panel display module to support 16 types of panels. You can select one of sixteen LCD panel types upon JP9 hardware jumper settings (see Chapter 2).

3-4-2 LCD Panel Interface Kit

The ROBO-505 provides one flat panel interface connector J15 (see Chapter 2) to connect panel interface kit for VGA, SVGA and XGA panel support. This installation skill is very simple and easy. Without any special tools, you only have to do board-to-board connection and lock up the screw. Please refer to the illustration below. It is an optional kit and acted as an intermediate interface between ROBO-505 and LCD-kit which is actually connected to LCD modules.

3-4-3 RTL8139 Fast Ethernet Controller

The on-board PCI device, LAN controller, adopts Realtek single chip Fast Ethernet Controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3x to support 10 Mb/s and 100 Mb/s operation. All of network activities will be reported on LED indicators.

3-4-4 On-board LED Indicator

The ROBO-505 provides two LED indicators to show on-line LAN status. These messages will give you a guide for troubleshooting.

LED1 (LAN Link Integrity LED)
ON : indicates link is good in either 10 or 100 Mbps
OFF : link is bad

LED2 (LAN Activity LED)
ON : indicates either transmit or receive activity
OFF : no activity

3-4-5 Drivers Support

ROBO-505 provides one CD-Title to support on-board VGA and Ethernet device drivers in various operating systems. This CD-Title includes two directories \Ethernet and \vga69000. Before installing the device drivers, please see the reference files in each sub-directory.

- Ethernet : RTL8139 Driver Disk Version 3.30
  Supports Win95, Win98, Winnt, Nt351, Linux, Sco,…etc.
  The “Mainmenu” file specifies Network drivers version for various O.S. environments.
- vga69000 : supports NT3.5, NT4.0, WIN95 and Win98 environment.

NOTE : For the installation of Ethernet driver in old version of NT environment, it is strongly recommended to use diskette instead of using the CD-Title directly due to a reported failure in switching CD-Title. Please copy files from the CD-Title to a diskette.

3-5 Watch Dog Timer Programming

There are two manners to activate the Watch-Dog Timer (WDT) function. One is to utilize hardware jumper setting and programmed by software command. After this feature is enabled, a system reset will be generated unless a application triggers the timer periodically within time-out period. This allows

the system to restart in an orderly way in case of any abnormal condition is found. Second one is to program super I/O W83977 chip to start WDT time-out counting. It is recommended to use first method. The second choice is comparatively difficult and complicated. In addition, you can also connect WDT output to NMI input by setting JP6 jumper to generate NMI event to support special interrupt service routine.

An optional two-port WDT is provided on ROBO-505. This WDT comes with 8 possible ranges of time intervals from 500 ms to 64 sec., which can be adjusted by setting jumper positions. It could be enabled and programmed by reading I/O port 0443H or 0433H to issue trigger continuously, and disabled by reading I/O port 0343H or 0033H. A tolerance of 30% timer limit must be considered. For instance, if the time-out interval is set to 1second, the WDT trigger command must be issued within 700ms at least.

The below example gives you a reference algorithm for WDT programming via I/O port 0433H and 0033H in your application program :

```
Enable WDT
        MOV     DX, 0433H
        IN      AL, DX
Re-trigger WDT
        MOV     DX, 0433H
        IN      AL, DX
Disable WDT
        MOV     DX, 0033H
        IN      AL, DX
```

NOTE : Please directly contact your technical specialist to get WDT programming information on super I/O chip for long time-out interval support from 0.5 minutes to 254.5 minutes.

CHAPTER 4

BIOS Setup Information

ROBO-505 is equipped with the AMI BIOS stored in Flash ROM. This BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, ROBO-505 communicates with peripheral devices and check its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start-up.

4.1 Entering Setup

Turn on or reboot the computer. When the message "Hit <DEL> if you want to run SETUP" appears, press <Del> key immediately to enter BIOS setup program.

If the message disappears before you respond, but you still wish to enter Setup, please restart the system to try "COLD START" again by turning it OFF and then ON, or touch the "RESET" button. You may also restart from "WARM START" by pressing <Ctrl>, <Alt>, and <Delete> keys simultaneously. If you do not press the keys at the right time and the system will not boot, an error message will be displayed and you will again be asked to,

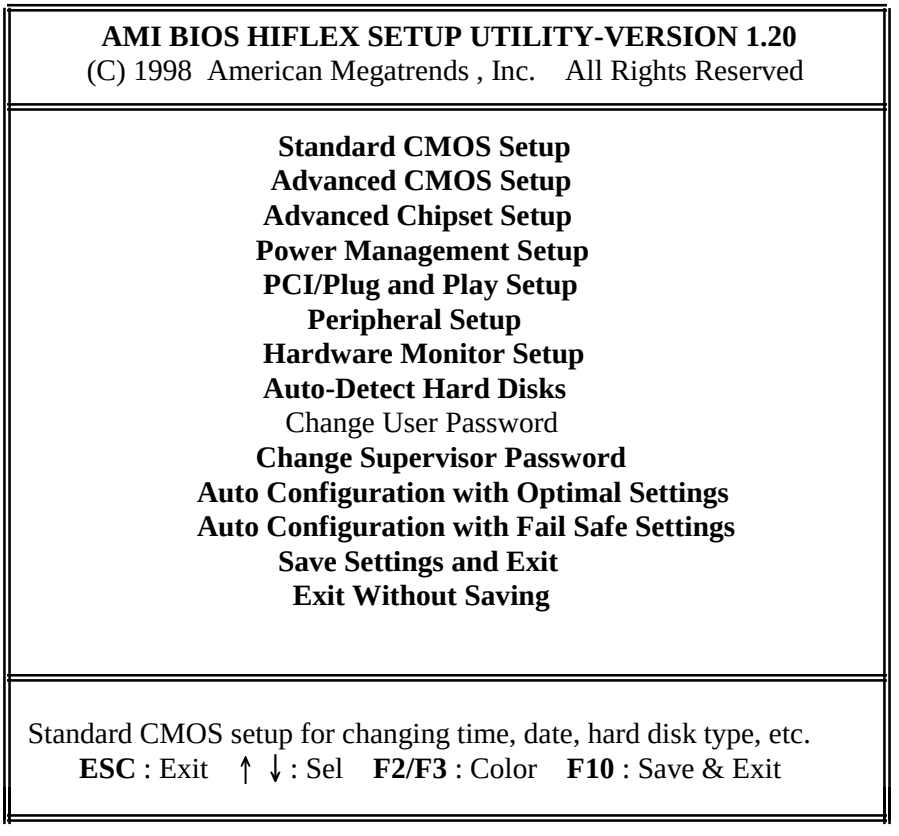
Press <F1> to Run SETUP or Resume

In HIFLEX BIOS setup, you can use the keyboard to choose among options or modify the system parameters to match the options with your system. The table below will show you all of keystroke functions in BIOS setup.

EDITING KEYS	FUNCTION
<Tab>	Move to the next field
← ↑ → ↓	Move the next field to the left, above, right, or below
<Enter>	Select in the current field
+ / –	Increments / Decrements a value
<Esc>	Close the current operation and return to previous level
<PgUp>	Returns to the previous option
<PgDn>	Advances to the next option
<F2>/<F3>	Select background color
<F10>	Show "Save current settings and exit (Y/N)" in main menu

4.2 Main Menu

Once you enter AMI BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from eleven setup functions and two exit choices. Use arrow keys to switch the items and press <Enter> to accept or enter the sub-menu.


AMI BIOS HIFLEX SETUP UTILITY-VERSION 1.20
(C) 1998 American Megatrends , Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Power Management Setup
PCI/Plug and Play Setup
Peripheral Setup
Hardware Monitor Setup
Auto-Detect Hard Disks
Change User Password
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit Without Saving
Standard CMOS setup for changing time, date, hard disk type, etc.
ESC : Exit ↑ ↓ : Sel F2/F3 : Color F10 : Save & Exit

NOTE : It is strongly recommended to reload Optimal Setting if CMOS is lost or BIOS is updated.

4.3 Standard CMOS Setup Menu

This setup page includes all the items in a standard compatible BIOS. Use the arrow keys to highlight the item and then use the <PgUp>/<PgDn> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it.

Follow command keys in CMOS Setup table to change **Date**, **Time**, **Drive type**, and **Boot Sector Virus Protection Status**.

Boot Sector Virus Protection Status

When enabled, this BIOS function will warn the user when any program attempts to write or format the boot sector and allows the user to intervene. The default setting is *Disabled*.

4.4 Advanced CMOS Setup Menu

This setup includes all of the advanced features in the system. The detail descriptions are specified as belows.

Boot Up Sequence

This category includes six items to determine which drive computer searches first for the Disk Operating System (DOS). The reference default setting is :

* 1st Boot Device	IDE-0
* 2nd Boot Device	Floppy
* 3rd Boot Device	ARMD-HDD
* 4th Boot Device	Disabled
* Try Other Boot Devices	Yes
* S.M.A.R.T. for Hard Disks	Disabled

The default ARMD (ATAPI Removable Media Device) emulation type is set to popular drive type; such as floppy for LS-120, hard disk for MO, and removable hard disk for IOMEGA Zip etc. There are many choices of booting devices to boot up system. User can select *Disabled*, *IDE-0*, *IDE-1*, *IDE-2*, *IDE-3*, *Floppy*, *ARMD-FDD*, *ARMD-HDD*, *CDROM*, *SCSI*, or *NETWORK*.

Quick Boot

Select *Enabled* to skip minor BIOS test items to get quick boot response. The default setting is *Disabled*.

Boot Up Num-Lock

Select "On" to enable numeric function of the numeric keypad, or "Off" to disregard it. The default setting is *On*.

PS/2 Mouse Support

Select "Enabled" to enable PS/2 mouse function, or "Disabled" to release IRQ12 interrupt for other ISA-bus I/O devices. The default setting is *Enabled*.

Primary Display

Chooses *Absent*, *VGA/EGA*, *CGA40x25*, *CGA80x25*, or *Mono* to meet your monitor type. If you select Absent, the "CMOS Display Type Wrong" message will be ignored for mismatched display card in CMOS setting. The default setting is *VGA/EGA*.

Password Check

This option enables the password checking when the system boots up or runs CMOS Setup. It only takes effect after setting Change Supervisor Password. The default setting is *Setup*.

Setup : This option will force system to check password before running Setup if you have already entered the current user password in "Change User Password". By that time, the system will be only able to boot but deny accessing Setup.

Always : Password prompt appears every boot-up. The system will not boot and deny access Setup with invalid password. The best way is to clear CMOS or try to reload BIOS Setup to boot up system.

Boot to OS/2, DRAM 64MB or Above

Set this option to *Yes* to permit BIOS to run properly if OS/2 or any other operating system that not support Plug and Play is to be run on this computer. If running OS/2

in a computer with 64MB or more of system memory, set this option to *Yes*. The optimal default setting is *No*.

Internal Cache

This option is used to enable or disable internal CPU L1 cache. Set this option to *WriteBack* to acquire better system performance. If you select *Disabled*, neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled. The final system performance will be slower than normal setting. The optimal default setting is *WriteBack*.

External Cache

This option specifies the caching algorithm used for L2 secondary (external) cache memory. Set this option to *WriteBack* to improve overall system performance. If you select *Disabled*, the external L2 cache will be not available and the system performance will be slower than normal setting. The optimal default setting is *WriteBack*.

System BIOS Cacheable

Set this option to "Enabled" to enhance system performance by shadowing and caching function , or ignore this BIOS shadow function by setting "Disabled". The optimal default setting is *Enabled*.

Shadow Memory (from address C000 – DFFF, 16K per segment)

Each of segments provides three options "Disabled", "Enabled", and "Cached" for faster adapter's ROM execution. However this shadow function is Chipset oriented and dependent on system hardware feature. The default setting for each of all segments are *Disabled* except for C000, C400 and C800. In general, this area C000 – CBFF (48KB) is allocated for VGA/Panel BIOS and set to *Cached* to get higher display performance by shadowing and caching feature. If user chooses *Enabled* setting, only BIOS shadow function is active.

4.5 Advanced Chipset Setup Menu

This setup is very important to keep system stability. If you are not technical person, do not attempt to change any parameters. The best way is to choose optimal default setting.

USB Function

This option will enable on-chip USB function to support USB (Universal Serial Bus) peripheral devices if a user chooses the "Enabled" setting. The default setting is *Disabled*.

USB Keyboard/Mouse Legacy Support

This feature will be automatically disabled and hidden if user chooses the "Disabled" setting from the foregoing **USB Function** option. Otherwise, enabling this option can support USB-keyboard or USB-Mouse without auxiliary driver under DOS environment.

SDRAM CAS Latency/ RAS to CAS

This option is used to control read data valid wait states after a read command has been issued. The "2/2" means a CAS# latency of 2 HCLKs and a RAS# to CAS# delay of 2 HCLKs is provided for all SDRAM cycles. Here HCLK means the CPU-clock period. The optimal default setting is *2/2*.

SDRAM Speculative Read Logic

This option relates to SDRAM pipeline function and Back-to-back Burst Read Page Hit . You can choose the "Disabled" setting for safe system performance or for low-speed SDRAM module. The *Disabled* setting means the next memory access can begin after the previous memory access is finished. However, you can select *Enabled* to optimize the memory data sequence to gain better SDRAM performance. This option is only effective if SDRAM system memory is installed in the computer. The default setting is *Disabled*.

Fast EDO Read Cycle Timing

This item is used to control EDO DRAM read timing. If you are using low-speed EDO DRAM (more than 70ns) or running higher CPU clock speed, it is necessary to select option "Disabled". Or you can select "Enabled" setting to get better system performance. This option is only effective if EDO system memory is installed in the computer. The default setting is *Disabled*.

DRAM Refresh RAS Cycles (HCLK's)

This option sets the number of DRAM refresh RAS cycles (in HCLKs). The settings are *4* or *5*. The default setting is *5*.

Memory Hole

This option allows the end user to specify the location of a memory hole for memory space requirement from ISA-bus cards. The settings are "Disabled", "512-640KB", "15-16MB", or "14-16MB". The default setting is *Disabled*.

8bit I/O Recovery Time

This option specifies the length of the delay (in SYSCLKs) inserted between consecutive 8-bit I/O operations. The settings are *Disabled, 8, 1, 2, 3, 4, 5, 6,* or *7* Sysclks. The optimal default setting is *Disabled*.

16bit I/O Recovery Time

This option specifies the length of the delay (in SYSCLKs) inserted between consecutive 16-bit I/O operations. The settings are *Disabled, 4, 1, 2,* or *3* Sysclks. The optimal default setting is *Disabled*.

4.6 Power Management Setup Menu

This APM (Advanced Power Management) determines how much power energy can be saved by setting below items to handle system power resource. The following descriptions will specify the detail meaning or definition of each item.

Power Management/APM

Using this feature to control system power resources. The default setting is *Enabled* to enable power management function and effective based on following parameter settings.

Green PC Monitor Power State

This option specifies the power state that the green PC-compliant video monitor enters when BIOS places it in a power savings state after the specified period of display inactivity has expired. There are three options “Stand By”, “Suspend”, and “Off” in this feature. The *Stand By* option is to turn off light power by handling of monitor signals. The other *Suspend* mode is to turn off heavy power. Another one, *Off* state, is really to turn off the power of the monitor. The default setting is *Off*.

Video Power Down Mode

This option specifies the power conserving state that the VESA VGA video subsystem enters after the specified period of display inactivity has expired. There are three options “Disabled”, “Stand By”, and “Suspend” in this field. The default setting is *Disabled*. If user select another options, it will be controlled by “Stand by Time out” and “Suspend Time out”.

Hard Disk Power Down Mode

This option specifies the power management state that the HDD enters after the specified period of hard drive inactivity has expired. It is the same as video power control. The default setting is *Disabled*. If user chooses *Stand By* or *Suspend*, it will depend on period of parameter “Stand By Time out”or “Suspend Time out”.

Stand by Time out (Minute)

This option specifies the length of the period of system inactivity while the computer is in Full-On power state before the computer is placed in Standby mode. When this length of time expires, the computer enters Standby Timeout state. In Standby mode, some power use is curtailed. The settings are *Disabled, 1, 2, 4, 8, 10,* and all ten minute intervals up to *60* min. The default setting is *Disabled*.

Suspend Time out (Minute)

This option is the same as **Stand by Time out** function. These two features will be enabled to monitor power of sub-items "VGA display", "Serial port", "Parallel Port", "Floppy", "Pri-HDD", and "Sec-HDD" independently. It is also used to control CPU throttle running function. All of sub-items will be ineffective in selection of disabling "Stand by Time out" or "Suspend Time out" even if it can be choosed by user in BIOS setup menu. The settings are Disabled, 1, 2, 4, 8, 10, 20, 30, 40, 50, and 60 min. The default setting is *Disabled*.

Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as duty cycle of the STPCLK# signal. This duty cycle indicates the percentage of time the STPCLK# signal is asserted while in the throttle mode. The settings are 0-12.5%, 12.5-25%, 25-37.5%, 37.5-50%, 50-62.5%, 62.5-75%, and 75-87.5%. The default setting *50-62.5%*.

Display Activity

This option specifies if BIOS is to monitor activity on the display monitor for power conservation purposes. If Display Activity is set to *Monitor* and the computer is in a power saving state, BIOS will watch for video display activity. The computer enters the full on-power state if any activity occurs. BIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ lines. If this option is set to *Ignore*, video display monitor activity is not monitored. The settings are *Monitor* (Enabled) or *Ignore* (Disabled). The default settings is *Ignore*.

Serial Port 1 & 2, Parallel Port, FDD, Pri/Sec HDD 0 & 1

When set to *Monitor*, these options enable event monitoring on the specified hardware device. If set to *Monitor* and the computer is in a power saving state, BIOS watches for activity on the device with specified IRQ line. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified device. No monitoring activity occurs if the option is set to *Ignore*. The settings for each of these options are *Monitor* or *Ignore*. The optimal default setting for Serial Port 1 & 2, Primary/Secondary master IDE, and System Thermal are set to *Monitor*. The rest of devices are default set to *Ignore*.

System Thermal

Set this option to *Monitor* for CPU thermal monitoring and speed down control. The system will automatically supervise the CPU environmental temperature. If the CPU surface temperature reachs the trip point set in Hardware Monitor Setup, the thermal detection will be effective and CPU will run in throttle control manner. The overall system performance will be reduced to half. This option is a trad-off of system performance and stability and configurable by user. The default setting is *Monitor*. You can choose *Ignore* setting to disable this thermal function.

4.7 PCI/Plug and Play Setup

This section describes configuring the PCI bus system. PCI (Peripheral Component Interconnect) is a system which allows I/O devices to operate at speeds nearing CPU's when they communicate with own special components. All of options described in this section are important and technical and it is strongly recommended that only experienced users could make any changes to the default settings.

Plug and Play Aware O/S

Set this option to "Yes" if the operating system installed in the computer is Plug and Play-aware. BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to "No" if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. ***You must set this option correctly, or PnP-aware adapter cards installed in your computer will not be configured properly***. The optimal default setting is *No*.

PCI Latency Timer (PCI Clocks)

This option is used to control PCI latency timer period (follow PCI clocks). Based on PCI specification 2.1 or later and PCI bus frequency in system, user can select different timer to meet their PCI bus environment. The default setting is *64* PCI clocks.

PCI VGA Palette Snoop

The option are “Disabled” and “Enabled”. Some display cards that are non-standard VGA such as graphics accelerations or MPEG video cards may not show colors properly. User can choose “Enabled” setting to correct this display mismatch problem and support any ISA adapter card installed in the computer requires VGA palette snooping. The default setting is *Disabled*.

PCI IDE BusMaster

Set this option to *Enabled* to specify that the IDE controller on the PCI local bus has bus mastering capability. The settings are *Disabled* or *Enabled*. The default setting is *Disabled*.

DMA Channel 0/1/3/5/6/7

These options specify if the named DMA Channel is available for using on the ISA/EISA bus or PnP (Plug & Play). The optimal default setting is *PnP*.

IRQ 3/4/5/7/9/10/11/12/14/15

These options specify the bus that the named interrupt request lines (IRQs) are used on. These options allow you to specify IRQs for use by legacy ISA adapter cards. These options determine if AMIBIOS should remove an IRQ from the pool

of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these PCI/ Plug and Play Setup to remove the IRQ by assigning option to *ISA/EISA* setting. All of IRQs presented in this Setup are configured as PCI/PnP. The optimal default setting is *PCI/PnP*.

4.8 Peripheral Setup

This section describes I/O resources assignment for all of on-board peripheral devices. Please be noticed that multiple IRQ assignments for serial port will result in IRQ conflict. You need to take care when IRQ option is fixed by manual operation.

On Board FDC

Three options are “Auto”, “Disabled”, and “Enabled”. If user wants to install different add-on super I/O card to connect floppy drives, set this field to *Disabled*. The default setting is *Auto*. It will call BIOS to automatically determine if the floppy controller should be enabled.

On Board Serial Port 1/Port 2

These fields control the resource assignments of two on-board serial interfaces SIO1 and SIO2. The following lists show current options in On Board Serial Port 1/ Port 2 :

Auto (default setting) → cannot set serial I/O resources by manual operation
Disabled → indicates on-board COM port function is ineffective
3F8h/COM1 → assign I/O address 3F8h to COM1 (default IRQ4)
2F8h/COM2 → assign I/O address 2F8h to COM2 (default IRQ3)
3E8h/COM3 → assign I/O address 3E8h to COM3
2E8h/COM4 → assign I/O address 2E8h to COM4

IR Port Support

It is recommended to assign serial port 3 for this option. The IR Mode Select has four settings IrDA, ASK IR, FIR, and CIR. The default setting for IR Port Support is set to *Auto*.

On Board Parallel Port

There are four optional items *Parallel Port Mode*, *EPP Version*, *Parallel Port IRQ*, and *Parallel Port DMA Channel* used to control on-board parallel port interface while user select I/O base address manually. The following lists are available options of on-board parallel port :

Auto (default setting) → user can not control all of LPT port I/O resources
Disabled → on-board parallel port function is ineffective and N/A
378h → locate IRQ7 for this default I/O address
278h → assign this I/O address to LPT1
3BCh → assign this I/O address to LPT1

◎ **Parallel Port Mode :**

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications. This Parallel Port Mode includes four options "Normal", "Bi-Dir", "EPP", and "ECP". The optimal default setting is *Bi-Dir*.

Setting	Description
Normal	Uni-direction operation at normal speed
Bi-Dir	Bi-direction operation at normal speed
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bidirectional Communication.

◎ **EPP Version :**

This option is only valid if the **Parallel Port Mode** option is set to *EPP*. This option specifies the version of the Enhanced Parallel Port specification that will be used by AMIBIOS. The settings are *1.9* or *1.7*. The optimal default setting is *1.9* .

◎ **Parallel Port IRQ :**

This option is only valid if the **Onboard Parallel Port** option is not set to *Disabled*. This option sets the IRQ used by the parallel port. The settings are *5* and 7. The optimal default setting is *7*.

◎ **Parallel Port DMA Channel :**

This option is only available if the setting of the **Parallel Port Mode** option is ECP. This option sets the DMA channel used by ECP-capable parallel port. The settings are *0*, *1*, or *3* (DMA channel 3). The optimal default setting is *3*.

On Board Serial Port 3/ Port 4

This option controls the resource assignments of on-board serial interface SIO3 and SIO4. The following lists show options in On Board Serial Port 3/ Port 4 :

Auto (default setting) → I/O resources will be assigned by system BIOS
Disabled → indicates this on-board COM port function is ineffective
3F8h/COM1 → assign I/O address 3F8h to COM1
2F8h/COM2 → assign I/O address 2F8h to COM2
3E8h/COM3 → assign I/O address 3E8h to COM3
2E8h/COM4 → assign I/O address 2E8h to COM4
250h/COM5 → assign I/O address 250h to COM5 **(For serial port4 only)**

The Serial Port3/ Port4 IRQ can be manually assigned by choosing *3, 4, 5, 9, 10, 11,* or *12*.

On Board IDE

This option specifies the on-board IDE controller channels that will be used. The settings are *Disabled*, *Primary*, *Secondary*, or *Both*. The optimal default setting is *Primary*. Because ROBO-505 only support one IDE interface, please don't attempt to select *Secondary* or *Both*.

4.9 Hardware Monitor Setup

This section describes thermal status and monitoring control for on-board hardware thermal device.

CPU Current Temperature

The option is used to display the current CPU surface temperature based on LM75 thermal detection. In general, the temperature tolerance will be within 3℃.

Basic Critical Temperature (BCT)

This option is used to set trip point of LM75 thermal detection. The settings are *Disabled*, *50* and all five degree intervals up to and including *95* ℃. The default setting is *75* ℃*/167* ℉.

4.10 BIOS POST Check Point List

AMIBIOS provides all IBM standard Power On Self Test (POST) routines as well as enhanced AMIBIOS POST routines. The POST routines support CPU internal diagnostics. The POST checkpoint codes are accessible via the Manufacturing Test Port (I/O port 80h).

Whenever a recoverable error occurs during the POST, the system BIOS will display an error message describing the message and explaining the problem in detail so that the problem can be corrected.

During the POST, the BIOS signals a checkpoint by issuing one code to I/O address 80H. This code can be used to establish how far the BIOS has executed through the power-on sequence and what test is currently being performed. This is done to help troubleshoot faulty system board.

If the BIOS detects a terminal error condition, it will halt the POST process and attempt to display the checkpoint code written to port 80H. If the system hangs before the BIOS detects the terminal error, the value at port 80H will be the last

test performed. In this case, the terminal error cannot be displayed on the screen. The following POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 07/15/95 version 6.24 (Enhanced).

Uncompressed Initialization Codes — The uncompressed initialization checkpoint hex codes are listed in order of execution :

Code	Description
D0	NMI is disabled. CPU ID saved. INIT code checksum verification will be started.
D1	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and going to 4GB flat mode.
D3	To start memory sizing.
D4	Returning to real mode. Executing any OEM patches and setting the stack next.
D5	Passing control to the uncompressed code in shadow RAM at E000:0000h. The INIT code is copied to segment 0 and control will betransferred to segment 0.

Code	Description
D6	Control is in segment 0. Next, checking if <Ctrl><Home> was pressed and verifying the system BIOS checksum. If either <Ctrl><Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
D7	To pass control to interface module.
D8	Main BIOS runtime code is to be decompressed.
D9	Passing control to the main system BIOS in shadow RAM next.

Bootblock Recovery Codes — The bootblock recovery checkpoint hex codes are listed in order of execution :

Code	Description
E0	The onboard floppy controller if available is initialized. Next, beginning the base 512KB memory test.
E1	Initializing the interrupt vector table next.
E2	Initializing the DMA and Interrupt controllers next.
E6	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
ED	Initializing the floppy drive.
EE	Start looking for a diskette in drive A: and read first sector of the diskette.
EF	A read error occurred while reading the floppy drive in drive A: .
F0	Next, searching for the AMIBOOT.ROM file in the root directory.
F1	The AMIBOOT.ROM file is not in the root directory.
F2	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3	Start reading AMIBOOT.ROM file, cluster by cluster.
F4	The AMIBOOT.ROM file is not the correct size.
F5	Next, disabling internal cache memory.
FB	Next, detecting the type of Flash ROM.
FC	Erasing the Flash ROM.
FD	Programming the Flash ROM
FF	Flash ROM programming was successful. Next, restarting the system BIOS.

Uncompressed Initialization Codes — The following runtime checkpoint hex codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Code	Description
03	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05	The BIOS stack has been built. Next, disabling cache memory.

Code	Description
06	Uncompressing the POST code next.
07	Next, initializing the CPU and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before the keyboard BAT command is issued.
0C	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary INIT after the K/B controller BATcommand test.
0F	The keyboard command byte is written next.
10	Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End> or <Ins> keys were pressed during power on.
12	To initialize CMOS if the *initialize CMOS RAM in every boot* is set or the <End> key is pressed. Going to disable DMA and Interrupt controllers.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh line is toggling. Checking the 15us on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration or setup required before interrupt vector initialization has completed. Interrupt vector init. is about to begin
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	To look for optional video ROM and give control.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed podt-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. Look for retrace checking next.
31	Display memory R/W test or retrace checking failed. To do alternate display retrace checking.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error message.

Code	Description
3A	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
40	Preparing the descriptor tables next.
42	Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory test.
48	Patterns written in base memory. Determining the amount of memory below 1MB next.
49	The amount of memory below 1MB has been found and verified. Determining the amount of memory above 1MB memory next.
4B	The amount of memory above 1MB has been found and verified. Checking for a soft reset and clearing the memory below 1MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4C	The memory below 1MB has been cleared via a soft reset. Clearing the memory above 1MB next.
4D	The memory above 1MB has been cleared via soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64KB memory size next.
4F	Memory size display started. This will be updated during memory test. Performing the sequential and random memory test next.
50	Memory testing/initialization below 1MB completed. Going to adjust displayed memory size for relocation and shadowing.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1MB next.
52	The memory above 1MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59	The *Hit <DEL>* message is cleared. The *<WAIT…>* message is displayed. Staring the DMA and interrupt controller test next.
60	The DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.

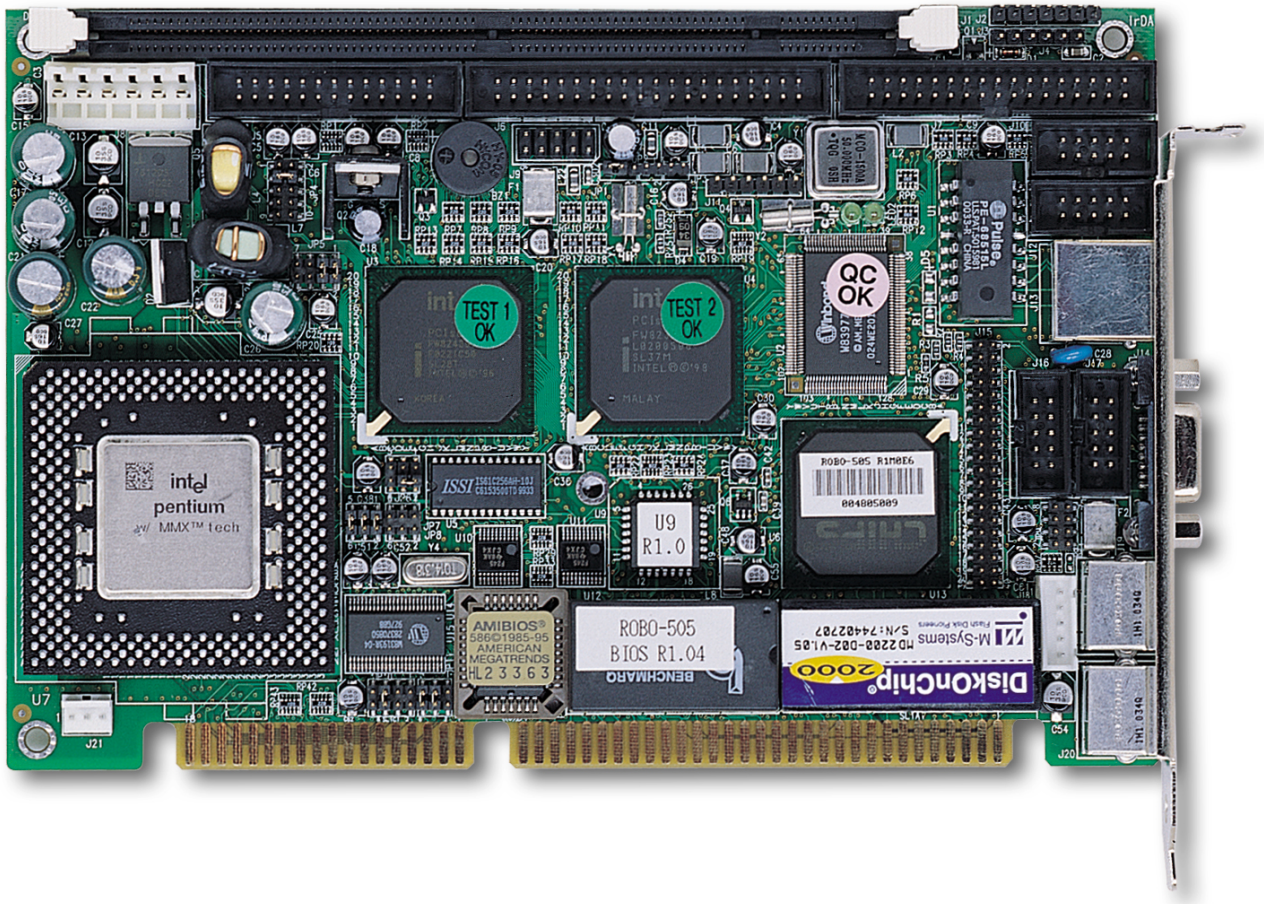
Code	Description
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	Command byte written, Global data init done. To check for lock-key.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing Setup next.
86	Password checked. About to do programming before setup.
87	The programming before Setup has completed. Uncompressing the Setup code and executing the AMIBIOS Setup utility next.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	The programming after Setup has completed. Displaying the power on screen message next.
8B	The first screen message has been displayed. The <WAIT…> message is displayed. Performaing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the Setup options next.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after setting the RS-232 base address. Performing any required Initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after the Coprocessor test is complete. Checking the extended Keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.

Code	Description
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary.
AC	Uncompressing the DMI data and initializing DMI POST next.
B0	The system configuration is displayed.
B1	Copying any code to specific areas.
00	Code copying to specific areas is done. Passing control to INT 19 h boot loader next.

4.11 Flash BIOS Utility

Utilize AMI Flash BIOS programming utility to update on-board BIOS for the future new BIOS version. Please contact your technical window to get this utility if necessary.

NOTE : Remark or delete any installed Memory Management Utility (such as HIMEM.SYS, EMM386.EXE, QEMM.EXE, …, etc.) in the CONFIG.SYS files before running Flash programming utility.


TEST 1
OK
TEST 2
OK
QC
OK
intel
pentium
w/ MMX™ tech
ISSI
U9
R1.0
ROBO-505 R1M0E6
004005089
AMIBIOS
586©1985-95
AMERICAN
MEGATRENDS
HL23363
ROBO-505
BIOS R1.04
BENCHMARQ
M-Systems
S/N:74402707
DiskOnChip 2000
IrDA
J21
J20

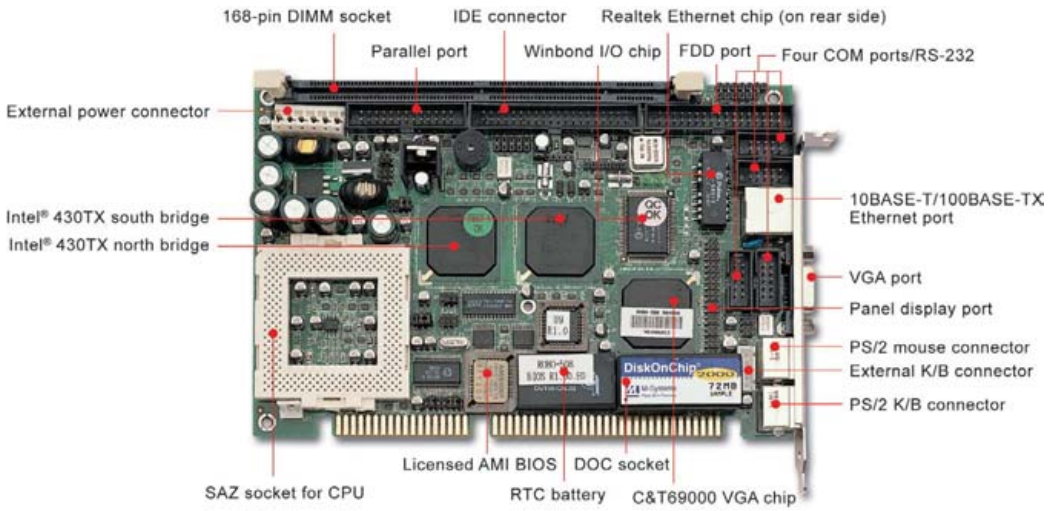
Portwell Half-Size Single Board Computer

Model	ROBO-636	ROBO-626	ROBO-616	ROBO-605	ROBO-505	ROBO-495
CPU	Intel Low power Pentium III	Intel Low power Celeron	FC-PGA Pentium III Celeron	FC-PGA Pentium III Celeron	P55C AMD K6 Cyrix 6x86	Cyrix 6x86
Front Side Bus	100MHz	100MHz	133MHz	66/100 MHz	N/A	N/A
Cache	Built-in CPU	Built-in CPU	Built-in CPU	Built-in CPU	512KB Pipeline	16KB L1
Max. Memory	1 DIMM/512MB	1 DIMM/512MB	1 DIMM/512MB	1 DIMM/256MB	1 DIMM/128MB	2 SIMM/64MB
Memory Type	SDRAM	SDRAM	SDRAM	SDRAM	EDO/SDRAM	FPM/EDO
ECC	NO	NO	NO	YES	NO	NO
BIOS	Award	Award	Award	AMI	AMI	Award
Chipset	Intel 815E	Intel 815E	Intel 815E	Intel 82440BX	Intel 82430TX	Cyrix Media GX
DiskOnChip	NO/CF Socket	NO/CF Socket	NO	Max. 288MB	Max. 288MB	Max. 288MB
CF SSD Support	YES	YES	YES	YES	YES	YES
PC-104	NO	NO	NO	NO	NO	NO
VGA/Panel	GMCH/NO	GMCH/NO	GMCH/NO	C&T 69000/YES	C&T 69000/YES	Built-in chipset/YES
SCSI	NO	NO	NO	NO	NO	NO
HDD Channel	2 IDE Ultra DMA/100	2 IDE Ultra DMA/100	2 EIDE Ultra DMA/100	1 EIDE Ultra DMA/33	1 EIDE Ultra DMA/33	1 EIDE Ultra DMA/33
FDD Drivers	2	2	2	2	2	1
Ethernet	10/100Base-T	10/100Base-T	YES	NO	YES	NO
USB Port	1 (2, factory optional)	1 (2, factory optional)	3	2	2	NO
ATX Control	YES	YES	YES	NO	NO	NO
On Board I/O	W83627HF	W83627HF	W83627HF	W83977ATF	W83977ATF	W83977ATF
Serial Port	2	2	2	2	4	2
Parallel Port	1	1	1	1	1	1
PS/2 K/B	YES	YES	YES	YES	YES	YES
PS/2 Mouse	YES	YES	YES	YES	YES	YES
WDT	YES	YES	YES	YES	YES	YES
H/W Monitoring	YES	YES	YES	YES	YES	YES
IrDA	YES	YES	YES	YES	YES	YES
Dimension (mm)	185(L) x 122(W)	185(L) x 122(W)	185(L) x 122(W)	185(L) x 122(W)	185(L) x 122(W)	185(L) x 122(W)

Please visit http://isc.portwell.com.tw for all CPU support type and speed

ROBO-505

Intel® Pentium® processor based half-sized ISA SBC with VGA/Panel and Fast Ethernet



FEATURE

- Reliable design for Socket 7 processor
- Intel® 82430TX PCI chipset, backed up by EID's long product life support
- PC100MHz SDRAM for cost effective memory support
- C&T 69000 and 2MB SDRAM provide a high performance, low power, highly integrated solution and versatile panel support
- On-board Intel® 10BASE-T/100BASE-TX Fast Ethernet for high speed data transfers
- Standard features for embedded system, like H/W monitoring, WDT, SSD and Wake-On-LAN
- One DOC socket for booting Windows NT directly

Ordering Information

Standard	**ROBO-505** Pentium® processor based half-sized ISA SBC with VGA/Panel and Fast Ethernet
Optional	**LCD-KIT-RS** Optional kit for TFT SVGA LCD panel **LCD-KIT-RX** Optional kit for XGA LCD panel

General

CPU	CPU & Package: Intel® P55C processor; AMD K6 processor; Cyrix 6x86MX processor FSB: 66MHz L2 Cache: 512KB pipeline burst SRAM
Chipset	Intel® 82430TX PCI chipset
Memory	Up to 128MB PC100 SDRAM on one 168-pin DIMM socket
BIOS	Award BIOS
Display	- C&T 69000 video display - 2MB display memory - Display resolution up to 1280x1024x8 bpp@60Hz - Support for CRT display or TFT/DSTN flat panel (optional) - D-sub 15-pin VGA connector at the rear panel
Ethernet	- Realtek 8139C PCI Ethernet - IEEE 802.3U auto-negotiation support - One RJ45 connector
Audio	N/A
SCSI	N/A
Expansion Interface	N/A
ISA Bus	64mA high driving ISA bus interface to backplane for legacy ISA slots
EIDE	Support two EIDE devices with Ultra DMA 33
Solid State Disk	DOC socket for up to 288MB
I/O	- On-board Winbond W83977ATF & W83877TF super I/O - Up to two floppy disk drives - Four serial, one parallel, one IrDA and two USB ports - Two 6-pin mini-DIN connectors for keyboard and mouse - One 5-pin header for external keyboard connection
ACPI Function	N/A
Hardware Monitoring	System monitor (fan, temperature, voltage)
Watchdog Timer	- Adjustable via hardware jumper setting from 0.5 sec. to 64 sec. - Programmable via software from 0.5 sec. to 254.5 min.
Power Requirement	+5V@5A; +12V@60mA; -12V@60mA (typ.)
Mechanical	Dimension: 185(L) x 122(W) / 7.3"(L) x 4.8" (W) PCB: 8-layer
Environmental	Operating Temperature: 0 to 55°C Storage Temperature: -20 to 75°C Relative Humidity: 5% to 95%, non-condensing
Approval	CE, FCC Class A
MTBF	143,032 hrs